Customer No.: 31561
Application No.: 10/605,401
Docket No.: 10587-US-PA

REMARKS

Present Status of the Application

The Office Action rejected claims 1, 3-6, 8-10, 12-14 and 16-18 and objected claims 2, 7, 11 and 15. Specifically, the Office Action rejected claim 1 under 35 U.S.C. 112 because it is unclear. The Office Action also rejected claims 1, 4-6 and 8 under 35 U.S.C. 102(b), as being anticipated by Lee (U.S. 6,228,700 B1). The Office Action also rejected claims 3 and 12 under 35 U.S.C. 103(a) as being unpatentable over Lee in view of Park (U.S. 6,071,799). The Office Action also rejected claims 9-10, 13-14, 16-18 under 35 U.S.C. 103(a) as being unpatentable over Lee in view of Nam (U.S. 5,728,627). The Office Action objected claims 2, 7, 11 and 15 as being dependent upon a rejected bas claim, but would be allowable if rewritten in independent form. After entry of the foregoing amendments, claims 2, 11 has been canceled, claims 1, 3-10, 12-18 remain pending in the present application, and reconsideration of those claims is respectfully requested.

Discussion of Office Action Rejections

Applicants respectfully traverse the 112 rejection of claim 1 because the step "planarizing the dielectric layer the cap layer of the gate structures and the bit line contact is exposed" is indefinite.

Applicants have amended said step of claim 1 to "planarizing the dielectric layer until the cap layer of the gate structures and the bit line contact ~~is~~ are exposed" to overcome the rejection.

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Applicants respectfully traverse the 102(b) rejection of claims 1, 4-6 and 8 because Lee. (U.S. 6,228,700 B1) does not teach every element recited in these claims.

In order to properly anticipate Applicants' claimed invention under 35 U.S.C 102, each and every element of claim in issue must be found, "either expressly or inherently described, in a single prior art reference". "The identical invention must be shown in as complete details as is contained in the .... claim. Richardson v. Suzuki Motor Co., 868 F. 2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989)." See M.P.E.P. 2131, 8th ed., 2001.

The present invention is in general related a method of forming bit line and bit line contacts in a memory device as claim 1 recites:

Claim 1. A method of forming bit lines and bit line contacts of a memory device, comprising the steps of:

providing a substrate having a plurality of gate structures thereon, wherein each gate structure comprises a gate dielectric layer, a gate conductive layer and a cap layer, and wherein a spacer is formed on each sidewall of the gate structure;

forming a conductive layer over the substrate to cover the gate structures;

planarizing the conductive layer until the cap layer of the gate structures is exposed;

removing a portion of the conductive layer but retaining the conductive layer between neighboring gate structures to form a bit line contact;

forming a dielectric layer over the substrate to cover the gate structures and the bit line contact;

planarizing the dielectric layer until the cap layer of the gate structures and the bit line contact are exposed;

forming a stop layer over the dielectric layer such that the bit line contact remain exposed; and

forming a bit line over the stop layer, wherein the bit line and the bit line contact are electrically connected.

Lee discloses a method for manufacturing DRAM including forming gates having gate oxide 300, a gate conductive layer 302 and barrier layer 304 on a substrate 200 (as shown in Fig 3A). Bit line plug 314 is formed inside the bit line contact opening, and an oxide layer 318 is formed on surface of the bit line plug 314 (as shown in Fig. 3C). A dielectric layer 320 is formed covering the bit line plug 314 and the oxide layer 318 and the dielectric layer 320 has an opening 322 therein exposing the bit line plug 314 (as shown in Fig. 3D). A bit line 324 is formed on the dielectric layer 320 and electrically connected with the bit line plug 314 through the opening 322. However, the method of Lee's reference lacks a step of forming a stop layer over the dielectric layer before the step of forming the bit line. Hence, Lee does not teach every element recited in these claim 1.

For at least the foregoing reasons, Applicant respectfully submits that independent claim 1 patently define over the prior art references, and should be allowed. For at least the same reasons, dependent claims 4-6, 8 patently define over the prior art as well.

Applicants respectfully traverse the rejection of claims 3 and 12 under 35 U.S.C. 103(a) as being unpatentable over Lee in view of Park (U.S. 6,071,799) because a prima facie case of obviousness has not been established by the Office Action. Applicants also respectfully traverse the rejection of claims 9-10, 13-14, 16-18 under 35 U.S.C. 103(a) as being unpatentable over Lee in view of Nam (U.S. 5,728,627) because a prima facie case of obviousness has not been established by the Office Action.

To establish a prima facie case of obviousness under 35 U.S.C. 103(a), each of three requirements must be met. First, the reference or references, taken alone or combined, must teach or suggest each and every element in the claims. Second, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skilled in the art, to combine the references in a manner resulting in the claimed invention. Third, a reasonable expectation of success must exist. Moreover, each of the three requirements must " be found in the prior art, and not be based on applicant's disclosure." See M.P.E.P. 2143, 8th ed., February 2003.

Applicants first submit that, as disclosed above, Lee fails to teach or suggest each and every element of claim 1, from which claims 3 and 9 depend. Because independent claim 1 patently define over the prior art references and should be allowed, its dependent claim 3 claiming further comprises forming a barrier layer over the substrate and the gate structure and dependent claim 9 claiming material constituting the bit line comprises tungsten should also be allowed.

Moreover, the present invention also discloses a method of forming bit line and bit line contacts in a memory device as claim 10 recites:

> Claim 10. A method of forming a memory device, comprising the steps of:
> providing a substrate comprising a memory cell region and a peripheral circuit region;
> forming a plurality of gate structures over the substrate within the memory cell region, wherein each gate structure comprises a gate dielectric layer, a gate conductive layer and a cap layer, and wherein a spacer is formed on each sidewall of the gate structures;
> forming a conductive layer over the substrate to cover the gate structures;
> planarizing the conductive layer until the cap layer of the gate structures is exposed;

removing a portion of the conductive layer but retaining the conductive layer between two neighboring gate structures to form a bit line contact;

forming a dielectric layer over the substrate to cover the gate structures and the bit lin contact;

planarizing the dielectric layer until the cap layer of the gate structures and the bit line contact are exposed;

forming a stop layer over the dielectric layer such that the stop layer exposes the bit line contact; and

forming a bit line over the stop layer so that a contact is also formed within the dielectric layer in the peripheral circuit region, wherein the bit line is electrically connected to both the bit line contact and the contact.

As discussed above, the method of Lee's reference lacks a step of forming a stop layer over the dielectric layer before the step of forming the bit line. Lee fails to teach or suggest the process of claim 10 comprising providing a substrate comprising a memory cell region and a peripheral circuit region and forming a bit line over the stop layer so that a contact is also formed within the dielectric layer in the peripheral circuit region, wherein the bit line is electrically connected to both the bit line contact and the contact.

For at least the foregoing reasons, Applicant respectfully submits that independent claim 10 patently define over the prior art references, and should be allowed. For at least the same reasons, dependent claims 12-18 patently define over the prior art as well.

CONCLUSION

For at least the foregoing reasons, it is believed that the pending claims 1, 3-10, 12-18 are in proper condition for allowance. If the Examiner believes that a telephone conference would

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expedite the examination of the above-identified patent application, the Examiner is invited to call the undersigned.

Respectfully submitted,

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Belinda Lee
Registration No.: 46,863

Jianq Chyun Intellectual Property Office
7th Floor-1, No. 100
Roosevelt Road, Section 2
Taipei, 100
Taiwan
Tel: 011-886-2-2369-2800
Fax: 011-886-2-2369-7233
Email: belinda@jcipgroup.com.tw
Usa@jcipgroup.com.tw